Design of Parallel Analog to Digital Converters for Ternary CMOS Digital Systems

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***Abstract* - Principles and possibilities for design and implementation of parallel analog to digital converters for application in ternary CMOS digital systems are considered and proposed in the paper. Such converters perform signal conversion from analog to ternary digital signal in CMOS ternary digital systems. First, general principle and structure for implementation and design of CMOS parallel analog to ternary digital converters are considered and proposed. Then, as an example and illustration of the design, concrete circuits for implementation of two digit parallel CMOS analog to ternary converters are proposed and described. Two types of such converters are considered and described: powerful type converters and simple type converters. All given solutions were analyzed using computer simulations. Descriptions and considerations were confirmed by the simulations.**

Keywords- analog to digital converters; ternary circuits and systems; CMOS logic circuits and systems; design of digital circuits and system; computer simulations

I. INTRODUCTION

The multiple-valued logic (MVL) circuits and systems have several important advantages comparing with the binary digital logic. The most important advantages are reduction in the number of interconnections required to implement the logic function, greater speed of logic and arithmetic operations, greater density of memorized information, better usage of transmission paths, decreasing of interconnections complexity and interconnections area, decreasing of pin number of integrated circuits and printed boards, possibilities for easier testing of digital systems [1-4].

Development of VLSI technologies is increased possibilities and interest for implementation of multiple-valued (MV) digital systems and circuits [1-4]. The greatest interest exists for research, development and implementation of ternary (logic basis 3) and quaternary (logic basis 4) MV circuits and systems [1-4]. The first designed and practically implemented have been ternary MV circuits and systems.

The multiple-valued systems, as well as the binary ones, also require and use analog to digital converters and digital to analog converters. So, there is need to develop and design appropriate converters for application in multiple-valued systems [5,6]. It is known that parallel analog to digital converters are the fastest converters.

The advantages and reasons for application of CMOS technology in the binary digital circuits and systems are very well known. All these advantages should be also kept in MV logic systems and circuits. There are also some advantages of CMOS technology that are important and characteristic for ternary logic. Since the first descriptions of ternary logic implementation the greatest interest exists for implementation in CMOS technology [1-4].

Principles and possibilities for development, design and implementation of parallel CMOS analog to digital converters for usage in ternary digital systems are proposed and described in this paper. First, general principle and structure for converters implementation and design are considered and proposed. Then, as the example and illustration of the converters design, the concrete circuits for two digit parallel CMOS analog to ternary converters are proposed and described. Two types of such converters are considered and described: so called powerful type converters and so called simple type converters. All proposed principles and solutions were analyzed and confirmed by computer PSpice simulations.

II. ANALOG TO TERNARY CONVERTER STRUCTURE

General principle and circuit structure for implementation of parallel CMOS binary to ternary converter are proposed and shown in Fig.1. There is one analog input signal (A_i) and there are m ternary digital signals (Y_i) at the outputs.

Proposed and shown structure in Fig.1 uses CMOS voltage comparator network at the input, CMOS binary encoder network and CMOS ternary output network at the outputs. The comparator network and binary CMOS encoder network are supplied by two supply voltages corresponding to two binary states: V_{SS} (binary logic 0) and V_{DD2} (binary logic 1). The ternary CMOS output logic network is supplied by three supply voltages corresponding to three ternary logic states: V_{SS} (ternary logic 0), V_{DD1} (ternary logic 1) and V_{DD2} (ternary logic 2).

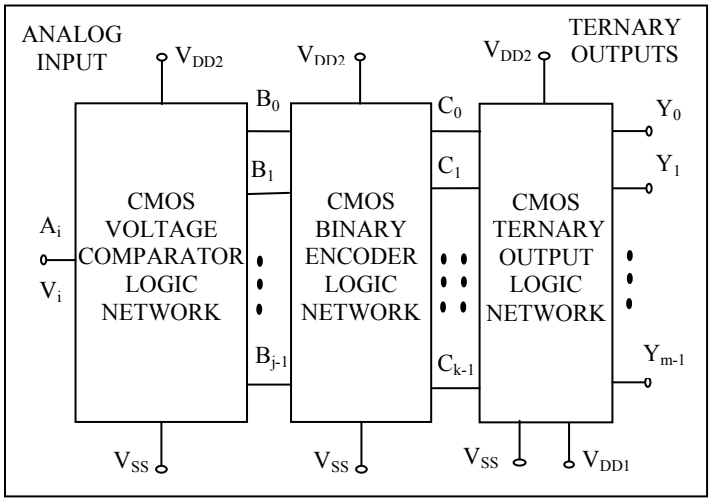

Fig.1. Structure of parallel CMOS analog to ternary converter.

The CMOS input comparator logic network performs comparison of input analog signal A_i (input voltage signal V_i) with appropriate threshold voltages. Since here is analog to ternary converter, there are existing 3^m-1 threshold voltages, where m is number of ternary digital outputs. Number of threshold voltages depends on converter resolution, i.e. on number of ternary digital outputs. The threshold voltages are in the middle between successive voltage levels of quantized analog signal. This network in principle can be realized in the same way as standard binary CMOS voltage comparator networks. For realization can be used standard CMOS binary voltage comparator circuits. This network gives binary output signals (B_i) with voltage levels of V_{SS} and V_{DD2}.

The CMOS binary encoder network performs encoding of the comparator network output signals (Bi) into appropriate binary signals (C_i) for control of ternary output network. This network in principle can be realized in the same way as standard binary CMOS encoder networks. For realization can be used standard CMOS binary logic circuits. It gives binary output signals (C_i) with voltage levels of V_{SS} and V_{DD2}.

The CMOS ternary output network generates needed output ternary signals (Y_i) according to states at the binary inputs (C_i), i.e. according to states at outputs of CMOS binary encoder logic network. Appropriate ternary output CMOS stages for every ternary CMOS output are in that network. It gives ternary output signals (Y_i) with voltage levels of V_{SS}, V_{DD1} and V_{DD2}.

In the proposed structure in Fig.1 there are one analog signal at the input and m ternary output signals at the outputs of the converter. It should be performed separately design and implementation of CMOS binary voltage comparator logic network, CMOS binary encoder network and CMOS ternary output logic network. The complexity of design and implementation of all three CMOS networks depend on number of ternary outputs m, and increases with increasing of m. Design of such converters includes determination of number of ternary outputs, selection of used output CMOS ternary stages (CMOS ternary output network), selection of used CMOS binary voltage comparators (CMOS binary voltage comparator network) and design of appropriate CMOS binary encoder network. After selection of output ternary CMOS stages and CMOS binary comparators the main task is to perform design of binary CMOS encoder logic network. It can be used standard methods of design of binary CMOS encoder logic circuits and methods for minimization of the network.

The proposed structure shown in Fig.1 is general one and gives possibility to develop and design CMOS analog to ternary converter with any number of ternary outputs, i.e. with any resolution. As an example and illustration of development and design of such converters, here will be shown way for design of two digit parallel CMOS analog to ternary converter.

III. TWO DIGIT PARALLEL CMOS ANALOG TO TERNARY CONVERTER DESIGN

Here will be shown and described way for design and implementation of parallel CMOS analog to ternary converters with two ternary outputs based on the proposed structure in Fig.1. Two types of such converters will be considered and described: powerful type converters and simple type converters. Based on the proposed structure it can be realized more different concrete solutions of CMOS parallel analog to ternary converters. Here will be proposed and described solutions that are appropriate for some concrete applications. First will be shown and described solutions of so called powerful type converters that have higher output power and use more MOS transistors. Then will be proposed way to obtain so called simple type converters that have smaller number of transistors and lower output power.

A. Powerful type converters

Proposed basic circuit of powerful type two digit CMOS parallel analog to ternary converter is shown in Fig.2. The circuit has one analog input (A_i) and two ternary outputs (Y_0 and Y_1). It uses simplified ternary CMOS output stages.

The CMOS voltage comparator network consists of eight (3^m-1 = 3^2-1 = 8, since number of converter outputs is m=2) voltage comparators (VC_i). Each comparator has appropriate threshold voltage (V_{Ri}) for comparison with input analog signal. The threshold voltages should be equal to the voltages that are in the middle between successive voltage levels of quantized analog signal. Each comparator compares the input analog signal with his threshold voltage and gives appropriate binary output signal B_i. For implementation of this CMOS comparator network can be used standard CMOS binary voltage comparator circuits.

The CMOS binary encoder network encodes the comparator network output signals (Bi) into appropriate binary signals (C_i) for control of ternary output network. Here there are eight encoder network input signals (B_i) and six output signals (C_i). This network can be realized in the same way as appropriate binary CMOS encoder network. Standard CMOS binary logic circuits can be used for implementation of the encoder network.

The CMOS ternary output network generates needed output ternary signals (Y_i) according to states at outputs of CMOS binary encoder logic network (C_i). Here is proposed appropriate ternary output network, i.e. appropriate ternary output CMOS stages for both ternary CMOS outputs. The

proposed output stages use only three MOS transistors, are the simplest ones and have the greatest output power.

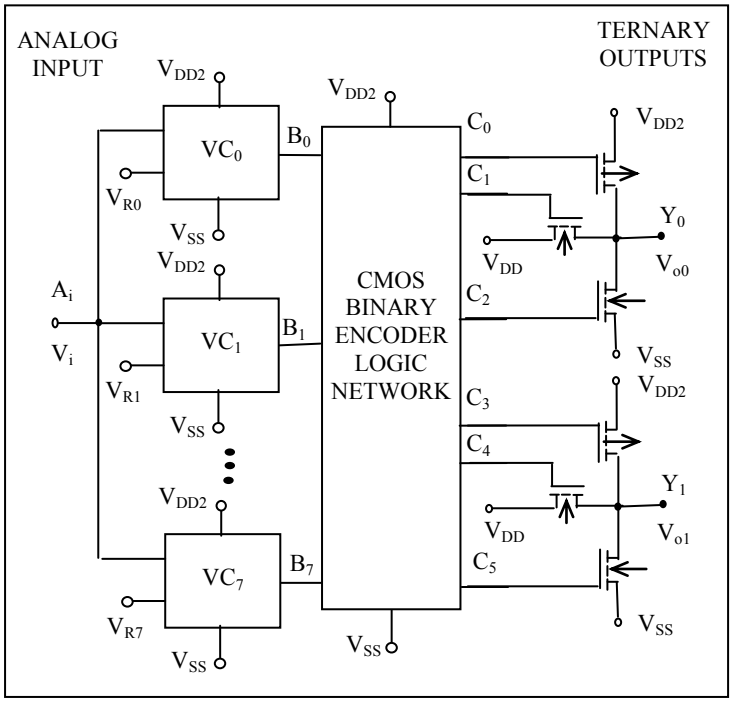

Fig.2. Two digit powerful type parallel CMOS analog to ternary converter.

Table I shows the way of operation of the two digit analog to ternary converter from Fig.2. All logic states are given in the ternary digital system.

$$C_1 = B_1\overline{B_0} + B_4\overline{B_3} + B_7\overline{B_6}\,, \quad (2)$$

$$C_2 = C_0 + C_1, \quad (3)$$

$$C_3 = B_1 + B_2, \quad (4)$$

$$C_4 = B_3\overline{B_2} + B_4\overline{B_3} + B_5\overline{B_4}\,, \quad (5)$$

$$C_5 = C_3 + C_4. \quad (6)$$

Based on the given expressions can be designed appropriate logic circuits proposed and given in Fig.3. Shown are designed encoder network and output stages of the converter. Standard binary CMOS inverting logic circuits (inverters, NAND and NOR logic circuits) are used for the design of the encoder network. Such is obtained analog to ternary converter of powerful type with minimized number of used transistors. All standard CMOS binary logic circuits are supplied by two supply voltages V_{SS} and V_{DD2}.

B. Simple type converters

Designs and implementations of analog to ternary CMOS converters with smaller total number of transistors can be obtained if we use different implementation of binary encoder network and different ternary output stages compared with the powerful type converters. Depending on the design of encoder network and ternary output stages can be obtained more different designs of complete analog to ternary converter.

Proposed circuit of output stage of simple type two digit CMOS parallel analog to ternary converter with minimal number of MOS transistors is proposed and shown in Fig.4.

TABLE I. LOGIC TABLE FOR TWO DIGIT CONVERTER

V_i	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	C_5	C_4	C_3	C_2	C_1	C_0	Y_1	Y_0
$V_i < V_{R0}$	2	2	2	2	2	2	2	2	2	0	2	2	0	2	0	0
$V_{R0} < V_i < V_{R1}$	2	2	2	2	2	2	2	0	2	0	2	2	2	0	0	1
$V_{R1} < V_i < V_{R2}$	2	2	2	2	2	2	0	0	2	0	2	0	0	0	0	2
$V_{R2} < V_i < V_{R3}$	2	2	2	2	2	0	0	0	2	2	0	2	0	2	1	0
$V_{R3} < V_i < V_{R4}$	2	2	2	2	0	0	0	0	2	2	0	2	2	0	1	1
$V_{R4} < V_i < V_{R5}$	2	2	2	0	0	0	0	0	2	2	0	0	0	0	1	2
$V_{R5} < V_i < V_{R6}$	2	2	0	0	0	0	0	0	0	0	0	2	0	2	2	0
$V_{R6} < V_i < V_{R7}$	2	0	0	0	0	0	0	0	0	0	0	2	2	0	2	1
$V_{R7} < V_i$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2

Based on the Table I, it can be designed appropriate CMOS binary encoder network. It can be obtained appropriate logic expressions for encoder logic outputs (C_i) as a function of encoder logic inputs (B_i). It can be shown that the expressions can be given in the next form:

$$C_0 = B_1B_0 + B_3\overline{B_2} + B_6\overline{B_5}\,, \quad (1)$$

The simple type converter with output stages given in Fig.4 has also analog input (A_i) and two ternary outputs (Y_0 and Y_1). It uses modified ternary CMOS output stages designed using serial and parallel connections of MOS transistors. This way of design enables to avoid usage of specially designed encoder CMOS network and to use only output signals of voltage comparators for direct control of transistors in ternary output

stages. This design drastically reduces total number of used MOS transistors comparing with the powerful type analog to ternary CMOS converter (Fig.2 and Fig.3). But, serial connections of MOS transistors in such designed ternary output stages increase propagation delay time and conversion time of the simple type converter compared with the powerful type one. It also creates different output powers and different delay times for different ternary output static states comparing with the powerful type converter, what is also a disadvantage of the simple type converters. Table I also shows the way of operation of the simple type two digit analog to ternary converter.

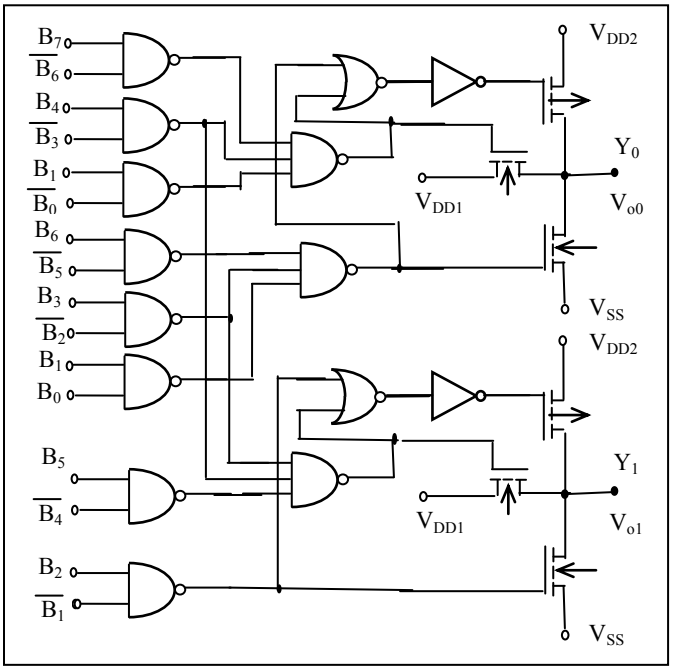

Fig.3. Encoder network and output stages of powerful type two digit analog to ternary converter.

C. *Simulation results*

Operations of proposed powerful type and simple type converters were analyzed by PSpice simulations. Technology parameters of one CMOS process [7] and supply voltages V_{SS}= -10V, V_{CC1}=0V, V_{CC2}=10V were used in simulations. Voltage CMOS comparator circuits as proposed and described in the paper [8], with appropriate designed threshold voltages, are used for design of CMOS voltage comparator network of analyzed analog to ternary converters. The voltage comparator circuits are based on the circuits proposed and described in the paper [9]. Timing diagrams of output ternary voltages as a function of input analog voltage for two digit powerful type converter, obtained by PSpice simulations are shown in Fig.5. At analog input was applied slow-changing signal for obtaining of all possible ternary states at outputs. Such is confirmed correct operation of the circuit and proper conversion of analog signal into ternary signals. By the simulations was also confirmed that the same signals (Fig.5) are valid also for the simple type two digit binary to ternary converter.

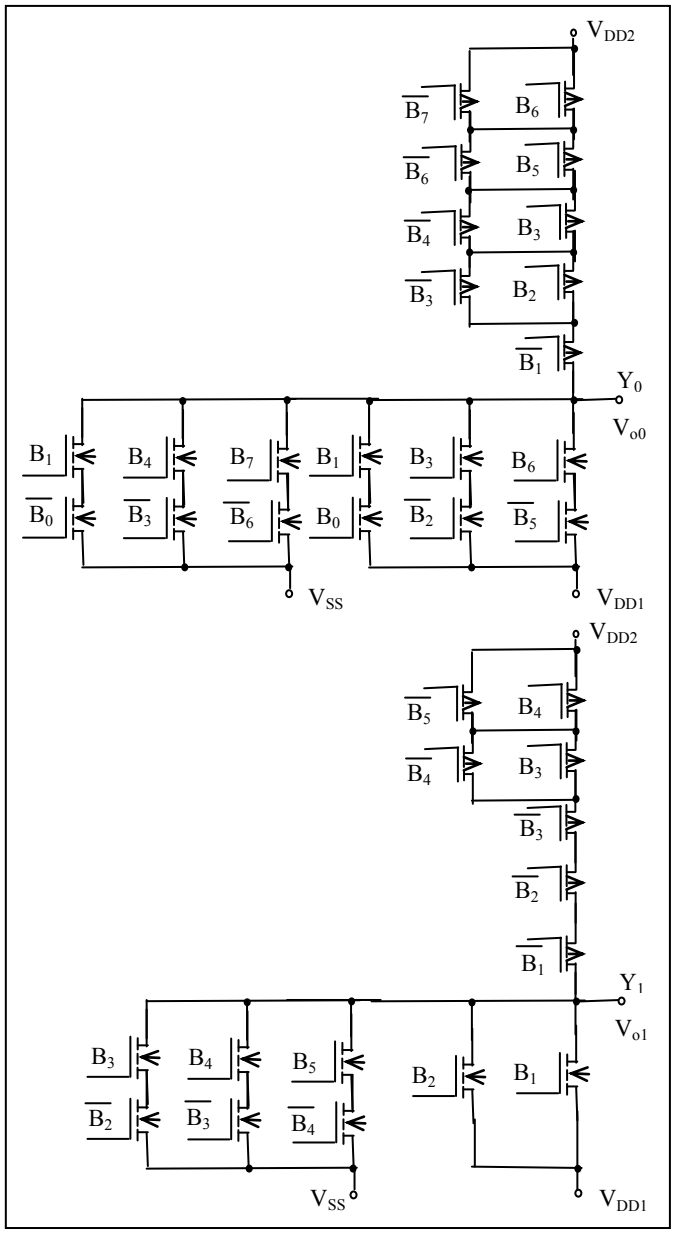

Fig.4. Output stages of simple type two digit analog to ternary converter.

The simulations confirm that the powerful type converters have smaller delay times and conversion times compared with simple type ones for applications with greater capacitive loads. In applications with smaller capacitive loads the simple type circuits have better this characteristics. Fig.6 shows conversion times (t_c) of the two digit powerful type and simple type analog to ternary converter as a function of capacitive load C_L obtained by PSpice simulations. In simulations were used the same technology parameters and the same supply voltages as in previous simulations and analysis. By full line are shown results for two digit powerful type converter and by dashed line are shown results for two digit simple type converter. It can be seen that powerful type converter has smaller conversion time for greater capacitive loads comparing with the simple type converter, what is the main advantage of the powerful type converter.

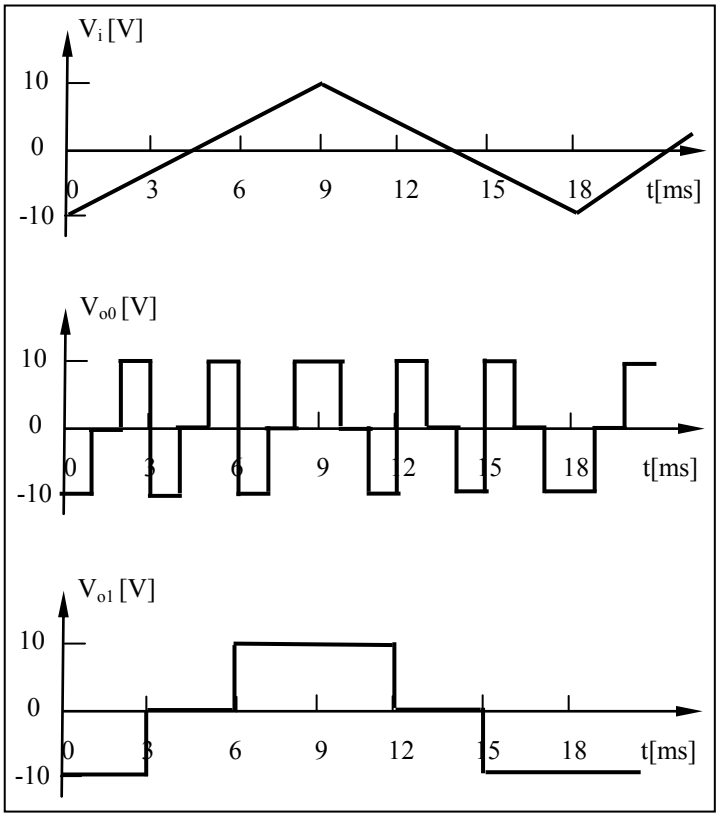

Fig.5. Timing diagrams of input analog signal and output ternary signals for powerful type analog to ternary converter.

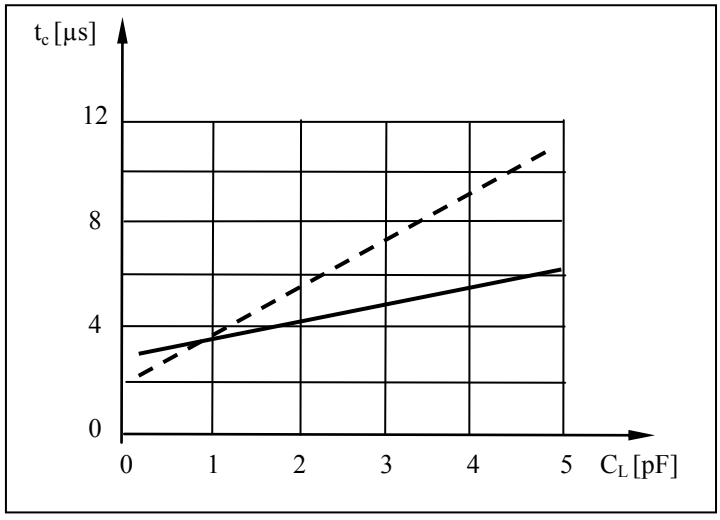

Fig.6. Conversion times of two digit analog to ternary converters as a function of capacitive load C_L.

It can be seen that the simple type analog to digital converter is simpler than the powerful type converter. It uses simpler CMOS binary encoder network (exactly do not use encoder network) and has smaller total number of MOS transistors. But, the simple type converter and converters obtained on such principle will generally have greater conversion time for greater loads than the powerful type converter.

IV. CONCLUSIONS

Well known advantages of MV digital systems are the main reasons for increase of interest for usage of such digital systems. Practically the greatest interest exists for ternary and quaternary MV systems. As well as in the binary digital systems, there is need to use analog to digital conversion and such converters in MV digital systems. Parallel analog to digital converters are the fastest ones.

Proposed principle and structure for design and implementation of parallel CMOS analog to ternary converters are clear and relatively simple. For implementation are used only standard MOS transistors, i.e. the standard MOS technology. Proposed and described principle enables design of converters with any (needed) number of ternary logic outputs, i.e. with any (needed) resolution, according to needed working conditions.

Described principles and solutions enable to obtain optimal converter depending on requirements of its application. The simple type converters are simpler and use smaller total number of transistors but have greater delay times and greater conversion times for greater loads. The powerful type converters are more complex and use more transistors but have smaller delay times and smaller conversion times for greater loads. The simple type converters should be used in applications with smaller loads and smaller needed working speeds. The powerful type converters should be used in applications with greater loads and greater needed working speeds.

In simulations were used parameters of one older CMOS technology process. The reason is to be possible to compare results of simulations and analysis with earlier obtained results for some other circuits.

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